

In re Patent Application of  
COFLER ET AL.  
Serial No. 10/082,816  
Filed: FEBRUARY 25, 2002

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Listing of the Claims:

This listing of claims replaces all prior versions and listing of claims in the application.

Claims 1-24 (canceled).

25. (Previously presented) A method of handling branching instructions using a processor comprising a program memory storing program instructions, and a processor core comprising a plurality of processing units and a central unit connected thereto, the central unit issuing instructions to the processing units based upon the program instructions, the method comprising:

- clocking the processor core with a clock signal;
- receiving a branching instruction in the course of a current clock cycle; and
- processing the received branching instruction in the course of the current clock cycle.

26. (Previously presented) A method according to Claim 25 wherein the processing units comprise a first processing unit including at least one address-pointing register; wherein a branching instruction uses the content of the at least one address-pointing register; and further comprising checking validity of the content of the at least one address-pointing register at the start of the current clock cycle so that the branching instruction is actually received by the central unit and processed if the content is

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declared valid, and, in an opposite case, the branching instruction is kept on hold for processing until the content is declared valid.

27. (Previously presented) A method according to Claim 26 further comprising recopying the content of the at least one address-pointing register into at least one corresponding duplicated address-pointing register; and wherein the checking is of the at least one corresponding duplicated address-pointing register.

28. (Previously presented) A method according to Claim 27 wherein every time the central unit receives a modifying instruction intended to modify the content of the at least one address-pointing register, and earlier in time than a branching instruction involving the at least one address-pointing register, the check of validity of the content of the corresponding duplicated register takes into account that this modifying instruction has or has not been processed by the first processing unit.

29. (Previously presented) A method according to Claim 28 wherein every time a modifying instruction intended to modify the content of the at least one address-pointing register is received by the central unit, a counter associated with the at least one address-pointing register is incremented; wherein every time this modifying instruction has been processed by the addressing unit, the counter is

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decremented; wherein when a branching instruction involving this register is ready to be issued to the central unit, the validity check includes the check on the value of the counter; and wherein the content of the duplicated register corresponding to said address-pointing register involved is declared valid if the value of the counter is equal to zero.

30. (Previously presented) A method according to Claim 25 wherein the at least one processing unit comprises a second processing unit including a guard-indication register; wherein in the presence of a guarded branching instruction, a check on validity of the guard indication assigned to the branching instruction and contained in the guard-indication register is carried out at a start of the current clock cycle; and wherein the guarded branching instruction is actually received by the central unit and processed, if the value of the corresponding guard indication is declared valid, and, in the opposite case, this guarded branching instruction is kept on hold for processing until the value of the corresponding guard indication is declared valid.

31. (Previously presented) A method according to Claim 30 wherein the content of the guard-indication register is recopied into a duplicated guard-indication register; wherein the check on the validity of the value of a guard indication is a check on the validity of the value of the corresponding guard indication contained in the duplicated guard-indication register.

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32. (Previously presented) A method according to Claim 31 wherein every time the central unit receives a modifying instruction intended to modify the value of a guard indication and earlier in time than a branching instruction guarded by the guard indication, the validity check on the value of the guard indication contained in the duplicated guard-indication register takes into account that this modifying instruction has or has not been processed by the second unit.

33. (Previously presented) A method according to Claim 32 wherein the processor core includes a FIFO memory associated with the second processing unit and intended to temporarily store instructions which are intended for the second processing unit; and wherein every time the central unit receives a modifying instruction intended to modify the value of a guard indication, a counter, clocked by the clock signal, is initialized at an initial value corresponding to a number of clock cycles for this modifying instruction to be stored in the FIFO memory; and wherein the validity check simultaneously takes into account the current value of the counter, the presence or the absence of the modifying instruction in the FIFO memory, and whether the guard-indication register has or has not been updated by this modifying instruction after the latter has left the FIFO memory.

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34. (Previously presented) A method according to Claim 33 wherein every time an instruction is extracted from the FIFO memory, a read counter is incremented; wherein every time an instruction is stored in the FIFO memory, a write counter is incremented; wherein every time an instruction modifying the value of a guard indication is stored in the FIFO memory, the current value of the write counter is stored in FIFO memory; and wherein determining of a still-present character of this modifying instruction in the FIFO memory includes the comparison of the memory-stored current value of the write counter with the current value of the read counter.

35. (Previously presented) A method according to Claim 34 wherein the read counter and the write counter have an identical binary size equal to a depth of the FIFO memory; wherein an overflow bit changing value every time the corresponding counter comes back to its initial value is associated with each counter; wherein every time an instruction modifying the value of a guard indication is stored in the FIFO memory, the current value of the overflow bit of the write counter is likewise stored in the FIFO memory; and wherein determining of the still-present character of this modifying instruction in the FIFO memory also includes the comparison of the current value of the overflow bit of the read counter with the memory-stored value of the overflow bit of the write counter.

36. (Previously presented) A method of handling

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branching instructions using a processor comprising a program memory storing program instructions, and a processor core comprising a plurality of processing units and a central unit connected thereto, the central unit issuing instructions to the processing units based upon the program instructions, the method comprising:

receiving at the central core a branching instruction during a current clock cycle and processing the received branching instruction during the current clock cycle.

37. (Previously presented) A method according to Claim 36 wherein the processing units comprise a first processing unit including at least one address-pointing register; wherein a branching instruction uses the content of the at least one address-pointing registers; and further comprising checking validity of the content of the at least one address-pointing register at the start of the current clock cycle so that the branching instruction is actually received by the central unit and processed if the content is declared valid, and, in an opposite case, the branching instruction is kept on hold for processing until the content is declared valid.

38. (Previously presented) A processor comprising:  
a program memory for storing program instructions;  
and  
a processor core being clocked by a clock signal and comprising a plurality of processing units and a central unit

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connected thereto, said central unit for issuing instructions to said processing units based upon corresponding program instructions;

said central unit comprising a branching module for receiving a branching instruction during a current clock cycle, and processing this branching instruction during the current clock cycle.

39. (Previously presented) A processor according to Claim 38 wherein a first processing unit includes at least one address pointing register; wherein a branching instruction uses the content of at least one of the address-pointing registers; wherein the central unit includes first validity-checking means able, at the start of the current cycle, to carry out a check on validity of the content of the at least one pointing register; and wherein the branching instruction is received by the central unit and processed if the content is declared valid, and, in an opposite case, the branching instruction is kept on hold in the program memory until the content is declared valid.

40. (Previously presented) A processor according to Claim 39 wherein said central unit comprises, for each address-pointing register, a duplicated address-pointing register a content of which is a copy of the corresponding address-pointing register; and wherein said first validity-checking means checks validity of the contents of the corresponding duplicated address-pointing register.

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41. (Previously presented) A processor according to Claim 40 wherein said central unit comprises first deriving means able, every time the central unit receives a modifying instruction intended to modify the content of an address-pointing register, and earlier in time than a branching instruction involving this address-pointing register, to derive a first flag signal representative that this modifying instruction has or has not been processed by said first unit.

42. (Previously presented) A processor according to Claim 41 wherein said first deriving means comprise:

a counter associated with each duplicated address-pointing register;

incrementation means able, every time a modifying instruction intended to modify the content of an address-pointing register is received by said central unit, to increment the counter associated with this register;

decrementation means, able to decrement the counter every time this modifying instruction has been processed by said first processing unit; and

comparison means able to compare a value of the counter with a zero value and to issue the first flag signal having a value which is representative of the result of the comparison;

wherein said first validity-checking means check the value of the first flag signal, the content of the duplicated register corresponding to said address-pointing register

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involved being declared valid if the value of the flag signal corresponds to a value of the counter equal to zero.

43. (Previously presented) A processor according to Claim 42 wherein a second processing unit includes a guard-indication register; wherein said central unit includes second validity-checking means able, in a presence of a guarded branching instruction, to carry out a check on validity of a value of the guard indication assigned to said branching instruction and contained in the guard-indication register, at the start of the current cycle; and wherein the guarded branching instruction is actually received by said central unit and processed if the value of the corresponding guard indication is declared valid, and, in the opposite case, this guarded branching instruction is kept on hold for processing until the value of the corresponding guard indication is declared valid.

44. (Previously presented) A processor according to Claim 43 wherein said central unit includes a duplicated guard-indication register a content of which is a copy of the guard-indication register; and wherein said second validity-checking means are able to check the validity of the value of a guard indication contained in the duplicated guard-indication register.

45. (Previously presented) A processor according to Claim 44 wherein said central unit includes second deriving

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means able, every time the central unit receives a modifying instruction intended to modify a value of a guard indication and earlier in time than a branching instruction guarded by the guard indication, to derive a second flag signal representative that this modifying instruction has or has not been processed by said second unit.

46. (Previously presented) A processor according to Claim 45 wherein said processor core includes a FIFO memory associated with said second processing unit and intended temporarily to store instructions which are intended for this second processing unit; and wherein said second deriving means comprise:

a counter clocked by the clock signal;

initialization means able, every time the central unit receives a modifying instruction intended to modify a value of a guard indication, to initialize said counter at an initial value corresponding to a number of clock cycles necessary for this modifying instruction to be stored in the FIFO memory; and

logic means receiving a first logic signal representative of a current value of said counter and receiving a second logic signal representative of the presence or the absence of the modifying instruction in the memory, and representative that the guard-indication register has or has not been updated by this modifying instruction after the instruction has left said FIFO memory;

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wherein said logic means issue the second flag signal; and

wherein said second validity-checking means check the value of the second flag signal.

47. (Previously presented) A processor according to Claim 46 wherein the second unit comprises control means able to determine a presence or absence of the modifying instruction in the memory, said control means comprising:

a read counter incremented every time an instruction is extracted from the second memory;

a write counter incremented every time an instruction is stored in the second memory;

a set of individual registers associated respectively with the set of guard indications;

a first control unit able, every time an instruction modifying a value of a guard indication is stored in the second memory, to store a current value of the write counter in a field of the individual register associated with this guard indication; and

a second control unit able to determine a still-present character of this modifying instruction in the memory, and including means of comparing the field of the individual register with a current value of the read counter.

48. (Previously presented) A processor according to Claim 47 wherein said write counter and read counter have an identical size equal to a depth of the second memory; wherein

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an overflow bit, changing value every time a corresponding counter comes back to its initial value, is associated with each counter; wherein each individual register further includes a one-bit auxiliary field; wherein the first control unit is able, every time an instruction modifying the value of a guard indication is stored in the second memory, also to store a current value of an overflow bit of the write counter in the auxiliary field of the corresponding individual register; wherein the second control unit includes auxiliary comparison means able to compare a current value of an overflow bit of the read counter with a content of the auxiliary field.

49. (Previously presented) A processor according to Claim 48 wherein the auxiliary comparison means include an EXCLUSIVE NOR logic gate.

50. (Previously presented) A processor according to Claim 38 having a decoupled architecture.